

### **REMARKS/ARGUMENTS**

Claims 1-21 are pending in the application. Applicants hereby requests further examination and reconsideration of the application, in view of the following remarks.

#### *Claim Rejections – 35 USC § 103*

The Patent Office rejected claims 1-21 under 35 U.S.C. § 103(a) as being unpatentable over Bereza, U.S. Patent No. 5,801,578 (Bereza) in view of Kuo, U.S. Patent No. 5,646,563. Applicant respectfully traverse this rejection for the following reasons.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. MPEP § 2143.03 citing *In re Ryoka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). See also *In re Wilson*, 165 U.S.P.Q. 494 (C.C.P.A. 1970). Moreover, when applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) the claimed invention must be considered as a whole; (B) the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) reasonable expectation of success is the standard with which obviousness is determined. See *MPEP § 2141 and Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 220 USPQ 182, 187 n.5 (Fed. Cir. 1986).

As noted by the Patent Office, Bereza fails to teach or suggest a constant current generator suitable for generating a current reference for providing a substantially constant gate-to-source bias for the P- and N-channel charge pump devices, as claimed in 1, 8 and 15, that the current reference generated by the constant current generator comprises a high power supply rejection for the P- and N- channel charge pump devices, as claimed in claims 2, 9 and 16, that the constant current generator comprises P- and N- channel bias devices, wherein the P- and N- channel charge pump devices function as current mirrors of the P- and N-channel bias devices, as claimed in claim 3, 10 and 17, or that the P- and N- channel charge pump devices have a substantially constant current, as claimed in claims 4, 11 and 18. FIG. 4 illustrates the generation of this current reference,  $I_{bias}$ , which flows between devices  $MP_{bias}$  and  $MN_{bias}$  and is generated by the  $Q_1$ ,  $Q_2$ ,  $MN_A$  and  $MN_B$  devices in conjunction with the resistor R. This bias generator voltage loop is embedded in the middle of the current

generator cell is not subject to the power rail transients. Any transients (glitches) on both power rails  $V_{DD}$  and  $V_{SS}$  will be attenuated by the common-mode rejection of the bias generator  $Q_1$ ,  $Q_2$ ,  $MP_A$ ,  $MP_B$ ,  $MN_A$  and  $MN_B$ . The  $I_{bias}$  current flows between the  $MP_{bias}$  and  $MN_{bias}$  drains. The resulting quiet bias current is then mirrored to the charge pump, as shown in FIG. 3A and 3B as item 318, and used for charging and discharging the capacitor  $C_c$  at the output. Consequently, the largest power rails glitch suppression happens in the  $I_{bias}$  current generator. Only second order glitch suppression is provided by the differential pairs  $MP_{2A}$ - $MP_{2B}$  and  $MN_{2A}$ - $MN_{2B}$  current steering. Bereza, on the other hand, teaches the use of a reference current  $I_r$  that is injected into the cascaded devices 310 and 312 and then is mirrored to the charge pump current sources 320 and 328 (see Bereza, FIG. 3). Consequently, any power rail transients will be superimposed on this current without any attenuation. Thus, unlike the present invention, Bereza does not employ common-mode rejection circuitry for the power rail noise suppression.

Kuo does not make up for this defect in Bereza, since Kuo, either alone or in combination with Bereza also fails to teach or suggest a constant current generator suitable for generating a current reference for providing a substantially constant gate-to-source bias for the P- and N-channel charge pump devices, wherein the current reference generated by the constant current generator comprises a high power supply rejection for the P- and N-channel charge pump devices, wherein the constant current generator comprises P- and N-channel bias devices, and wherein the P- and N- channel charge pump devices function as current mirrors of the P- and N-channel bias devices, or wherein the P- and N- channel charge pump devices have a substantially constant current. Instead, Kuo applies the charge/discharge control through the P-channel 332 and N-channel 328 devices. The controlling digital signals for both devices are generated by the phase detector 310. There are two significant problems with this approach. First, full digital transients ( $V_{SS}$ - $V_{DD}$ ) on the gates of devices 332 and 320 will directly couple via Gate-Drain overlap capacitances of devices 322 and 328 into the output  $V_{out}$  as a noise current. Second, the noise transients at the  $V_{DD}$  power rail are again directly coupled as an error current into the output  $V_{out}$ . This noise current is additive to the reference current  $I_1$ . Consequently, unlike the present invention, Kuo fails to address the power rails glitch noise. Moreover, the Patent Office has

provided no reason, suggestion, or motivation from the prior art for modifying the teaching of Bereza and Kuo to achieve Applicant's invention.

Accordingly, it is submitted that the Patent Office has failed to establish *prima facie* obviousness of claims 1-21 under 35 U.S.C. § 103(a). Withdrawal of the rejection of these claims is therefore respectfully requested.

With respect to claims 5-7, 12-14 and 18-21, the rejections contain only the general statements that the elements of Applicant's invention claimed in these claims which are not recited by Bereza or Kuo are "inherent" in the teaching these reference or are simply "known." With respect to the assertion by the Patent Office that the elements of Applicant's invention not recited by Bereza or Kuo are inherent in their teaching, it is noted that

[T]he doctrine of inherency is available only when the prior inherent event can be established as a certainty. . . . A prior inherent event cannot be established based upon speculation or where a doubt exists.

*Ethyl Molded Products Co. v. Betts Package Inc.*, 9 U.S.P.Q. 2d 1001, 1032-33 (E.D. Ky. 1988). Moreover,

In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teaching of the applied prior art.

*Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). However, the Patent Office has furnished no arguments or references providing rationale or evidence tending to show that the elements of Applicant's invention claimed in claims 4-6, 11-13 and 17-20 not recited by Bereza or Kuo are inherent in their teaching.

With respect to the assertion by the Patent Office that the elements of Applicant's invention claimed in claims 7, 14 and 21 that not recited by Bereza or Kuo are known, the Examiner has provided no references supporting his position. As the Office is well aware, Applicant is required to seasonably challenge statements that are not supported on the record, and failure to do so will be construed as an admission by Applicant that the statement is true. M.P.E.P. § 2144.03. Therefore, in accordance with Applicant's duty to seasonably challenge such unsupported statements, the Patent Office is hereby requested to cite a reference supporting his position that the elements of Applicant's invention not taught by Bereza or

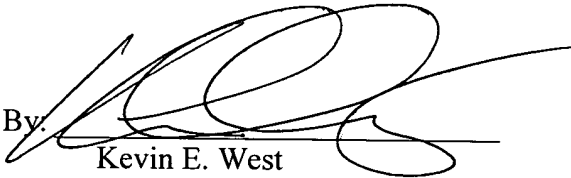
Kuo are known. If the Patent Office is unable to provide such a reference, and is relying on facts within the Examiner's own personal knowledge, Applicant hereby requests that such facts be set forth in an affidavit from the Examiner under 37 C.F.R. § 104(d)(2).

**CONCLUSION**

The application is respectfully submitted to be in condition for allowance of all claims. Accordingly, notification to that effect is earnestly solicited.

Respectfully submitted on behalf of  
LSI Logic Corporation,

Dated: August 12, 2003

By:   
Kevin E. West  
Reg. No. 43,983

SUITER • WEST PC LLO  
14301 FNB Parkway, Suite 220  
Omaha, NE 68154  
(402) 496-0300      telephone  
(402) 496-0333      facsimile